

2N3304

PNP HIGH-SPEED SWITCH

SILICON PLANAR EPITAXIAL TRANSISTOR

The 2N3304 is a very high speed PNP silicon epitaxial PLANAR device intended primarily for use in high speed logic application. A 500 mc minimum f_T and a 30 nsec maximum τ_s make it an ideal alternative to germanium devices for applications requiring the greater margin of reliability afforded by its silicon PLANAR construction.

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature

-65°C to +200°C

Operating Junction Temperature

200°C Maximum

Lead Temperature (Soldering, 60 sec time limit)

300°C Maximum

Maximum Power Dissipation

Total Dissipation at 100°C Case Temperature

0.5 Watt

[Notes 2 and 3]

at 25°C Ambient Temperature

0.3 Watt

[Notes 2 and 3]

Maximum Voltages and Current

 V_{CB0} Collector to Base Voltage

-6.0 Volts

 V_{CE0} Collector to Emitter Voltage [Note 4]

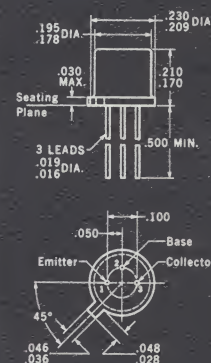
-6.0 Volts

 V_{EB0} Emitter to Base Voltage

-4.0 Volts

PHYSICAL DIMENSIONS

in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Collector internally connected to case
Package weight is 0.43 gram

ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
τ_s	Charge Storage Time [Note 6]		22	30	nsec	$I_c \approx 10 \text{ mA}$ $I_{B1} \approx 10 \text{ mA}$ $I_{B2} \approx -10 \text{ mA}$
t_{on}	Turn On Time [Note 6]		27	60	nsec	$I_c \approx 10 \text{ mA}$ $I_{B1} \approx 0.5 \text{ mA}$
t_{off}	Turn Off Time [Note 6]		34	60	nsec	$I_c \approx 10 \text{ mA}$ $I_{B1} \approx 0.5 \text{ mA}$ $I_{B2} \approx -0.5 \text{ mA}$
h_{fe}	High Frequency Current Gain ($f = 100 \text{ mc}$)	5.0	7.0			$I_c = 10 \text{ mA}$ $V_{CE} = -5.0 \text{ V}$
h_{FE}	DC Pulse Current Gain [Note 5]	30	63	120		$I_c = 10 \text{ mA}$ $V_{CE} = -0.3 \text{ V}$
h_{FE}	DC Pulse Current Gain [Note 5]	20	50			$I_c = 50 \text{ mA}$ $V_{CE} = -1.0 \text{ V}$
h_{FE}	DC Pulse Current Gain [Note 5]	15	60			$I_c = 1.0 \text{ mA}$ $V_{CE} = -0.5 \text{ V}$
$V_{CE}(\text{sat})$	Collector Saturation Voltage	-0.05	-0.15		Volts	$I_c = 1.0 \text{ mA}$ $I_B = 0.1 \text{ mA}$
$V_{CE}(\text{sat})$	Collector Saturation Voltage	-0.07	-0.16		Volts	$I_c = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
$V_{CE}(\text{sat})$	Collector Saturation Voltage	-0.2	-0.5		Volts	$I_c = 50 \text{ mA}$ $I_B = 5.0 \text{ mA}$

Additional Electrical Characteristics on page 2

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NOTES:

- (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 200°C/watt (derating factor of 2.0 mW/°C); junction-to-ambient thermal resistance of 583°C/watt (derating factor of 1.72 mW/°C).
- (4) This rating refers to a high-current point where collector-to-emitter voltage is lowest. For more information send for Fairchild Publication APP-4.
- (5) Pulse Conditions: length = 300 μsec ; duty cycle = 1%.
- (6) See switching circuit for exact values of I_C , I_{B1} and I_{B2} .

FAIRCHILD

SEMICONDUCTOR

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

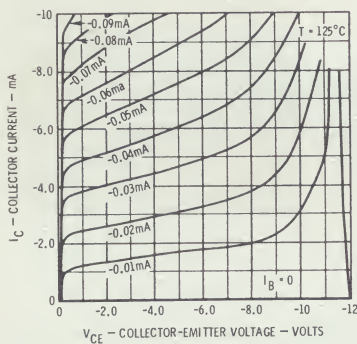
FAIRCHILD TRANSISTOR 2N3304

ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

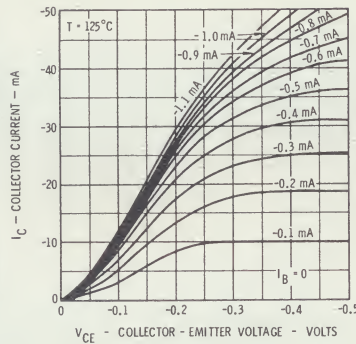
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$h_{FE} (-55^{\circ}\text{C})$	DC Pulse Current Gain [Note 5]	12	33			$I_C = 10 \text{ mA}$ $V_{CE} = -0.3 \text{ V}$
$V_{BE} (\text{sat})$	Base Saturation Voltage	-0.7	-0.76	-0.8	Volts	$I_C = 1.0 \text{ mA}$ $I_B = 0.1 \text{ mA}$
$V_{BE} (\text{sat})$	Base Saturation Voltage	-0.8	-0.88	-1.0	Volts	$I_C = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
$V_{BE} (\text{sat})$	Base Saturation Voltage		-1.1	-1.5	Volts	$I_C = 50 \text{ mA}$ $I_B = 5.0 \text{ mA}$
$V_{CE} (\text{sat}) (125^{\circ}\text{C})$	Collector Saturation Voltage	-0.09	-0.23		Volts	$I_C = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
I_{CES}	Collector Reverse Current	0.003	10		nA	$V_{CE} = -3.0 \text{ V}$ $V_{EB} = 0$
$I_{CES} (125^{\circ}\text{C})$	Collector Reverse Current	0.001	10		μA	$V_{CE} = -3.0 \text{ V}$ $V_{EB} = 0$
C_{ob}	Output Capacitance	1.9	3.5		pf	$V_{CB} = -5.0 \text{ V}$ $I_E = 0$
C_{TE}	Emitter Transition Capacitance	1.8	3.5		pf	$V_{EB} = -0.5 \text{ V}$ $I_E = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	-6.0			Volts	$I_C = 100 \mu\text{A}$ $I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	-6.0			Volts	$I_C = 100 \mu\text{A}$ $I_B = 0$
$V_{CEO} (\text{sust})$	Collector to Emitter Sustaining Voltage [Notes 4 and 5]	-6.0			Volts	$I_C = 10 \text{ mA}$ $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	-4.0			Volts	$I_E = 100 \mu\text{A}$ $I_C = 0$

TYPICAL COLLECTOR AND BASE CHARACTERISTICS*

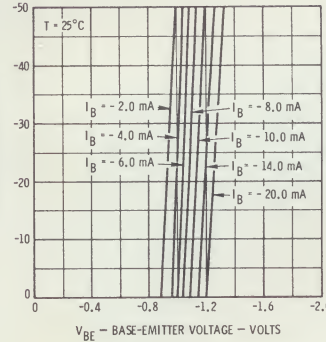
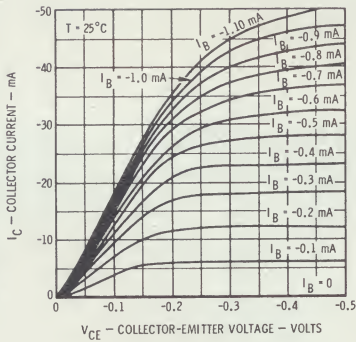
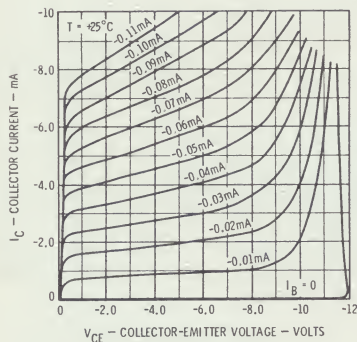
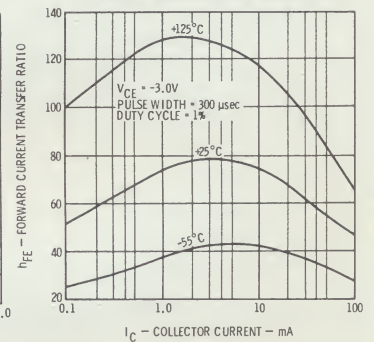
ACTIVE REGION



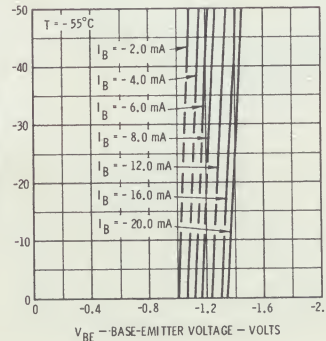
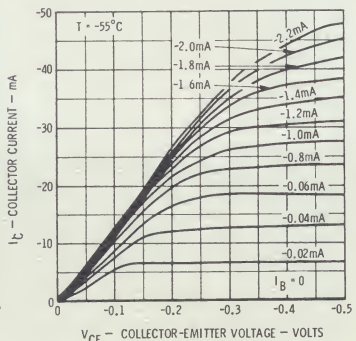
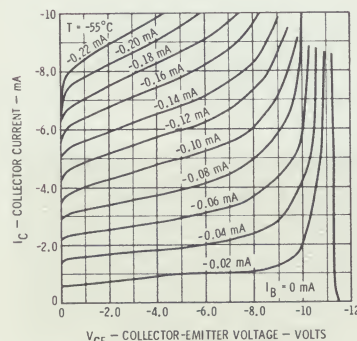
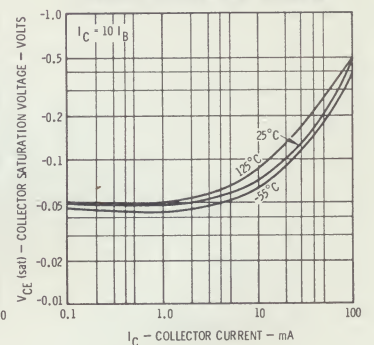
SATURATION REGION



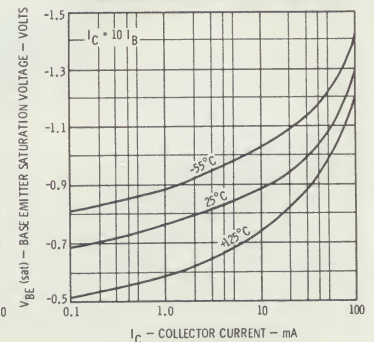
PULSED DC CURRENT GAIN VERSUS COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



* Single family characteristics on Transistor Curve Tracer.

The figure displays 16 graphs for the 2N4350 JFET, organized in a 4x4 grid. Each graph has a title and specific axes.

- Row 1:**
 - Graph 1:** Collector Reverse Current versus Reverse Bias Voltage. Y-axis: I_{CES} - Collector Reverse Current - μA . X-axis: V_{CE} - Collector-Emitter Voltage - Volts. $T_A = 25^\circ C$.
 - Graph 2:** Collector Reverse Current versus Ambient Temperature. Y-axis: I_{CES} - Collector Reverse Current - μA . X-axis: T_A - Ambient Temperature - $^\circ C$. $V_{CE} = -3.0V$.
 - Graph 3:** Capacitances versus Reverse Bias Voltage. Y-axis: CAPACITANCE - pF. X-axis: REVERSE BIAS VOLTAGE - Volts. Curves for C_{GB} at $f = 0$ and C_{FE} at $f = 0$.
 - Graph 4:** Contours of Constant Gain Bandwidth Product (f_T). Y-axis: V_{CE} - Collector Voltage - Volts. X-axis: I_C - Collector Current - mA. Contours for 100 mc, 50 mc, 30 mc, 20 mc, 10 mc, 5 mc, 3 mc, 2 mc, 1 mc.
- Row 2:**
 - Graph 5:** Switching Times versus Collector Current. Y-axis: SWITCHING TIMES - nsec. X-axis: I_C - Collector Current - mA. Curves for t_s , t_r , t_d , t_f . $I_C = 20 I_{B1} = 20 I_{B2}$, $V_{CC} = -2V$.
 - Graph 6:** Switching Times versus Ambient Temperature. Y-axis: SWITCHING TIMES - nsec. X-axis: T_A - Ambient Temperature - $^\circ C$. Curves for t_s , t_r , t_d , t_f . $I_C = 10$ mA, $I_{B1} = I_{B2} = 0.5$ mA, $V_{CC} = -1.5V$.
 - Graph 7:** Delay Time versus Turn On Base Current and Reverse Base Emitter Voltage. Y-axis: $V_{BE}(0)$ - Reverse Base-Emitter Voltage - Volts. X-axis: I_{B1} - Turn On Base Current - mA. Curves for 20 nsec, 10 nsec, 8 nsec, 5 nsec, 3 nsec. $I_C = 10$ mA, $V_{CC} = -2V$.
 - Graph 8:** Rise Time versus Collector and Turn On Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_C - Collector Current - mA. Curves for 2 nsec, 5 nsec, 10 nsec, 20 nsec. $V_{CC} = -2V$.
- Row 3:**
 - Graph 9:** Storage Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 10 nsec, 20 nsec, 30 nsec, 40 nsec, 50 nsec. $I_C = 1$ mA, $V_{CC} = -2V$.
 - Graph 10:** Storage Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 10 nsec, 15 nsec, 20 nsec, 30 nsec, 40 nsec, 50 nsec. $I_C = 10$ mA, $V_{CC} = -2V$.
 - Graph 11:** Storage Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 10 nsec, 20 nsec, 30 nsec, 40 nsec, 50 nsec. $I_C = 30$ mA, $V_{CC} = -2V$.
- Row 4:**
 - Graph 12:** Fall Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 20 nsec, 30 nsec, 40 nsec, 50 nsec. $I_C = 1$ mA, $V_{CC} = -2V$.
 - Graph 13:** Fall Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 2 nsec, 3 nsec, 4 nsec, 5 nsec, 6 nsec, 8 nsec, 10 nsec, 20 nsec. $I_C = 10$ mA, $V_{CC} = -2V$.
 - Graph 14:** Fall Time versus Turn On and Turn Off Base Currents. Y-axis: I_{B1} - Turn On Base Current - mA. X-axis: I_{B2} - Turn Off Base Current - mA. Curves for 2 nsec, 3 nsec, 4 nsec, 5 nsec, 6 nsec, 8 nsec, 10 nsec, 20 nsec. $I_C = 30$ mA, $V_{CC} = -2V$.

TURN ON AND TURN OFF TEST CIRCUIT

Circuit diagram showing a JFET in a common-emitter configuration. Input: $V_{in} = +5.0V$, P.W. = 100 nsec, $Z_{in} = 50 \Omega$, $t_r, t_f < 1.0$ nsec. Biasing: $V_{BB} = -6.0V$, $V_{CC} = -1.5V$, $5K \Omega$ base resistor, 130Ω collector resistor. Output: To Sampling Scope, $Z_{in} > 100 K \Omega$, $t_r < 1.0$ nsec. Test conditions: $I_C = 10$ mA, $I_{B1} = 0.5$ mA, $I_{B2} = -0.5$ mA.

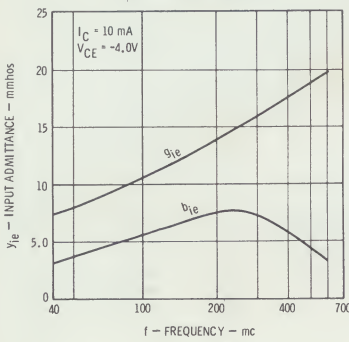
CHARGE STORAGE TIME TEST CIRCUIT

Circuit diagram showing a JFET in a common-emitter configuration. Input: $V_{in} = +9.0V$, P.W. = 100 nsec, $Z_{in} = 50 \Omega$, $t_r < 1.0$ nsec. Biasing: $V_{BB} = -10V$, $V_{CC} = -3.0V$, 510Ω base resistor, 390Ω collector resistor, 770Ω emitter resistor. Output: To Sampling Scope, $Z_{in} > 100 K \Omega$, $t_r < 1.0$ nsec. Test conditions: $I_C = 10$ mA, $I_{B1} = 10$ mA, $I_{B2} = -10$ mA.

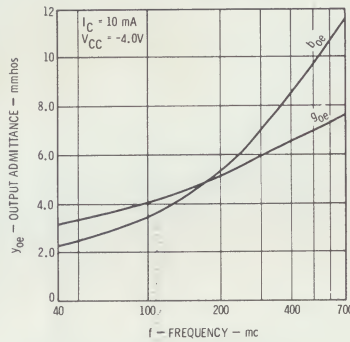
FAIRCHILD TRANSISTOR 2N3304

TYPICAL COMMON EMITTER "Y" PARAMETERS

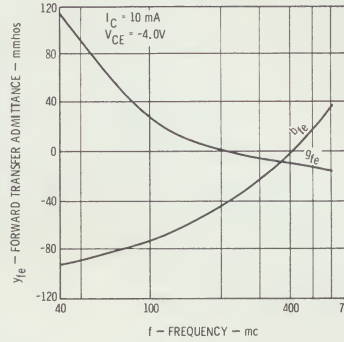
INPUT ADMITTANCE VERSUS
FREQUENCY-OUTPUT
SHORT CIRCUIT



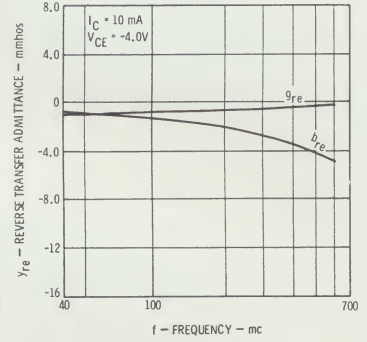
OUTPUT ADMITTANCE VERSUS
FREQUENCY-INPUT
SHORT CIRCUIT



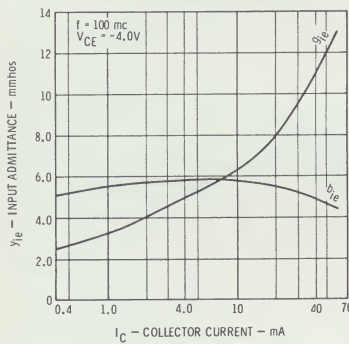
FORWARD TRANSFER ADMITTANCE
VERSUS FREQUENCY-OUTPUT
SHORT CIRCUIT



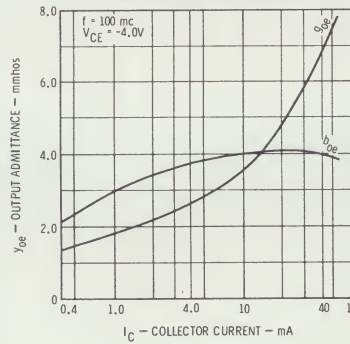
REVERSE TRANSFER ADMITTANCE
VERSUS FREQUENCY-INPUT
SHORT CIRCUIT



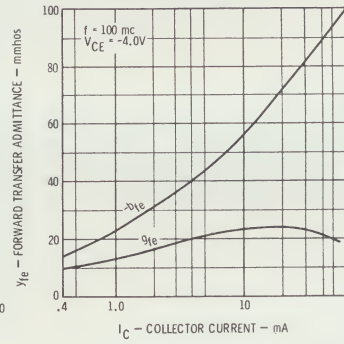
INPUT ADMITTANCE VERSUS
COLLECTOR CURRENT —
OUTPUT SHORT CIRCUIT



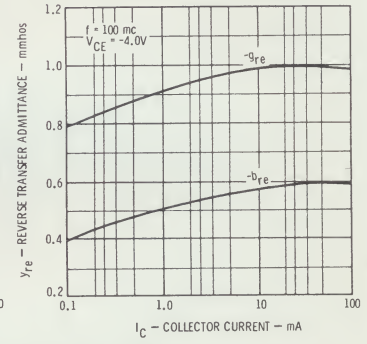
OUTPUT ADMITTANCE VERSUS
COLLECTOR CURRENT —
INPUT SHORT CIRCUIT



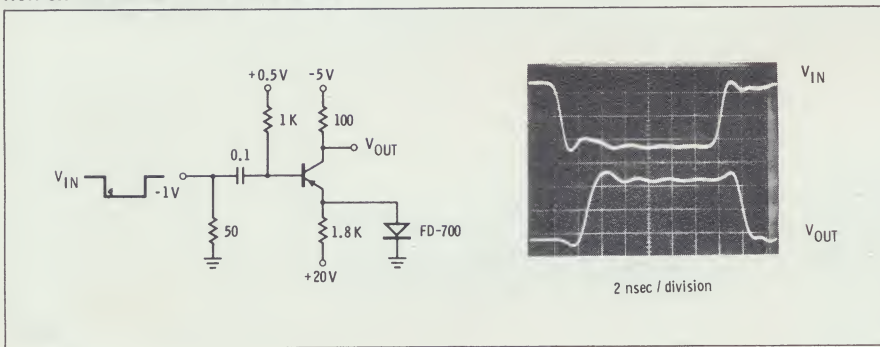
FORWARD TRANSFER ADMITTANCE
VERSUS COLLECTOR CURRENT —
OUTPUT SHORT CIRCUIT



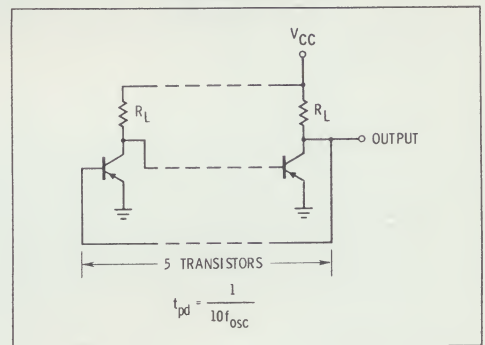
REVERSE TRANSFER ADMITTANCE
VERSUS COLLECTOR CURRENT —
INPUT SHORT CIRCUIT



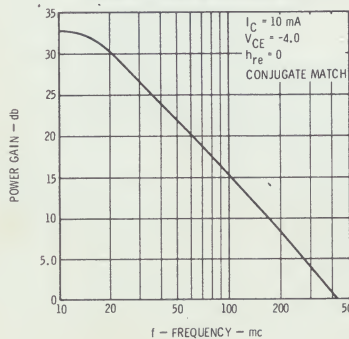
NON SATURATED SWITCHING PERFORMANCE



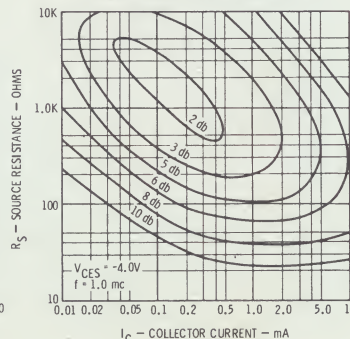
FIVE STAGE RING OSCILLATOR FOR MEASUREMENT OF PROPAGATION DELAY



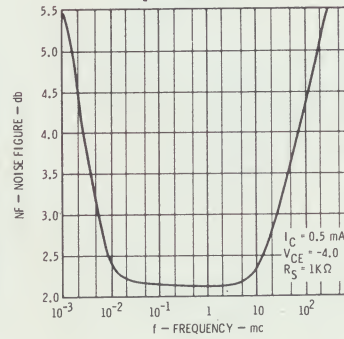
IDEALIZED SMALL SIGNAL POWER
GAIN VERSUS FREQUENCY



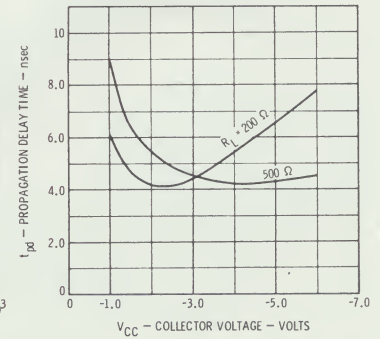
NOISE FIGURE VERSUS
SOURCE RESISTANCE
AND COLLECTOR CURRENT



NOISE FIGURE VERSUS
FREQUENCY



PROPAGATION DELAY TIME
VERSUS
COLLECTOR SUPPLY VOLTAGE



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